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COMPUTER BASED MODELLING OF DDS WITH POLYNOMIAL APPROXIMATION

Marinov Angel, Technical University of Varna, a.marinov@tu-varna.bg

Abstract: The current paper presents an implementation of series based direct digital synthesis for underwater distance measurement with improved polynomial coefficients and decreased number of computation operations. A computer based model representing the real work of a digital signal processor implementing the presented algorithm is shown. The results are analyzed and compared. It is proven that the presented model is suitable for testing and implementing direct digital synthesis algorithms.

Keywords: direct digital synthesis, distance measurement, digital signal processing

КОМПЮТЪРНО БАЗИРАНО МОДЕЛИРАНЕ НА ДИРЕКТЕН ЦИФРОВ СИНТЕЗ СЪС ПОЛИНОМИАЛНА АПРОКСИМАЦИЯ

Ангел Маринов, Технически Университет Варна, a.marinov@tu-varna.bg

Абстракт: Настоящата статия представя имплементирането на директен цифров синтез базиран на изчислителен ред. Целевото приложение на директният цифров синтез е в акустична система за измерване на разстояние. Представен е модел на изчислителната процедура при реализацията ѝ със сигнален процесор. Получените чрез модела резултати са анализирани и сравнени. Показано е че модела е подходящ при имплементирането на разгледаната система чрез специфични микроконтролери и сигнални процесори.

Ключови думи: директен цифров синтез, измерване на разстояние, цифрова обработка на сигнали

Introduction

The Direct Digital Synthesis (DDS) is a technique for generating a high quality sine wave through a digitally defined frequency. The software implementation of DDS based on digital signal processor has two main versions – using ROM table of the sine wave and series approximation of the sine wave. The first one is most common and faster, but due to the restricted ROM table size, the spurious free dynamic range (SFDR) of the spectrum of the synthesized signal is also limited. The series based DDS however eliminates the restrictions of the ROM table. A drawback is the bigger number of required mathematical operations, which results in lower sampling frequency [1].

DDS is most commonly an integrated block of complex devices, i.e. underwater distance measurement system [2,3]. Practically the implementation of the complete system before

studying the possibilities for optimization of the algorithms is not recommended. Therefore the development of computer model and simulation of the possible results will reduce the cost and time for implementation in the real device.

The current paper presents a generalized simulation model of series based DDS with a 5th order optimized polynomial.

Algorithm

Based on previous researches an optimized 5th order polynomial approximation is suggested in [4, 5]. It may be represented by the following equation:

$$\sin(\alpha) = \alpha - a_3\alpha^3 + a_5\alpha^5 \qquad (1)$$

where a_i, i=3,5, are the coefficients of the sinus approximation. The values of the coefficients are determined by using optimization algorithms (steepest ascent or genetic algorithms optimization). The range of the argument is $[-\pi/2, \pi/2]$ and thus the even-order components of the polynomial are eliminated.

Based on the presented polynomial a simulation model for software DDS, representing the work of a microcontroller or digital signal processor is suggested. The model includes the parameters of the selected microprocessor and demonstrates the algorithms implementation. In addition, the model allows with minimum experimental data to include the exact time of calculation and extraction of each of the generated signal samples. Thus the developed model can be easily included in complex systems which will allow the direct evaluation of its parameters.

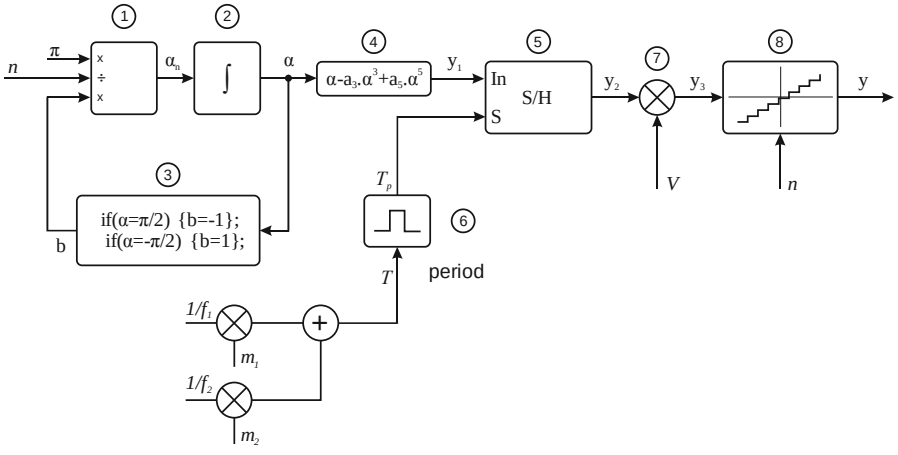


Fig. 1 Series based DDS with improved 5th order polynomial

Figure 1 represents a generalized block diagram of the series based DDS with improved 5th order polynomial. The model is built from the following blocks:

1. Phase step forming – in this block, the phase step, set for the sine function, is defined. The phase step is formed through π/n, where n defines the needed resolution of the generated

signal and it must be a number between 6 and 16. The step may be with positive or negative sign depending on the work of the phase accumulator – summation or subtraction respectively. Thus in mode of summation the phase step has positive sign for the interval [0, π] and negative sign for the interval [π, 2π].

2. Phase accumulation – the phase accumulator forms the phase argument α, through which the output signal based on the sine function is synthesized. Depending of the sign of the phase, it sums a number in the interval [–π/2, π/2] and subtracts in the interval [π/2, –π/2]. For obtaining the needed output frequency, the phase step must be equal to:

$$p = \frac{1}{f \cdot 2^n} \qquad (2)$$

Thus the phase accumulator represents an integrator with limits [-π/2, π/2]. The limits are defined by the block for sign alternation.

3. Overflow check– here the program statement is defined using C programing language:

$$\text{if } (\alpha = \frac{\pi}{2}) \text{ \{b=-1\}; if}(\alpha = \frac{-\pi}{2}) \text{ \{b=1\};} \qquad (3)$$

The statement is true when the phase argument α has reached π/2 or –π/2, which changes the value of local variable b to –1 or 1.

4. Phase to signal converter - formed through the block 1, 2 and 3 phase angle α is set to the block for calculating the sine function trough polynomial approximation. Here the preferred polynomial for calculating the output sine signal is used (in the present case the function (1)). The output of this block is the preferred signal y1. These four blocks represent the ideal implementation of the series based DDS algorithm. In order to account for the effects of the microcontroller parameters block 5, 6, 7 and 8 are added.

5. Sample and hold block – its purpose is to hold the output value for the time corresponding to the number of cycles a microprocessor needs for calculating and leading out the output sample of the signal. The delay time is formed in block 6 of the presented model.

6. Period set – this block sets the time for which block 5 will hold the last calculated value of the signal y_1. The time is formed by the following equation:

$$T = \frac{m_1}{f_1} + \frac{m_2}{f_2} \qquad (4)$$

Where:

- m_1 is the number of instructions needed for calculating one sample
- f_1 is the frequency with which the microprocessor calculates the samples

- m_2 is the number of instructions for leading out the value to the output port
- f_2 is the working frequency of the peripheral devices - for the common microcontrollers $f_1 = f_2$, but for the digital signal processors often $f_1 > f_2$.

7. Block for equating the level of the output signal with the level of the digital to analogue converter – the calculated value y2 is multiplied with the reference voltage of the digital to analogue converter. Thus the output signal y3 is formed.

8. Block for quantizing the output signal - here the output value is quantized the number of samples is reduced to the number available from the used digital to analogue converter.

Implementations

1. MATLAB model

The presented model is implemented in Simulink, MATLAB as is shown in figure 2. The blocks corresponding to the scheme in figure 1 are specified as follows: phase step forming; phase accumulator, which includes the phase accumulation block and the overflow check; phase to signal converter in which is also included and the period set block; sample and hold; digital to analogue converter (DAC).

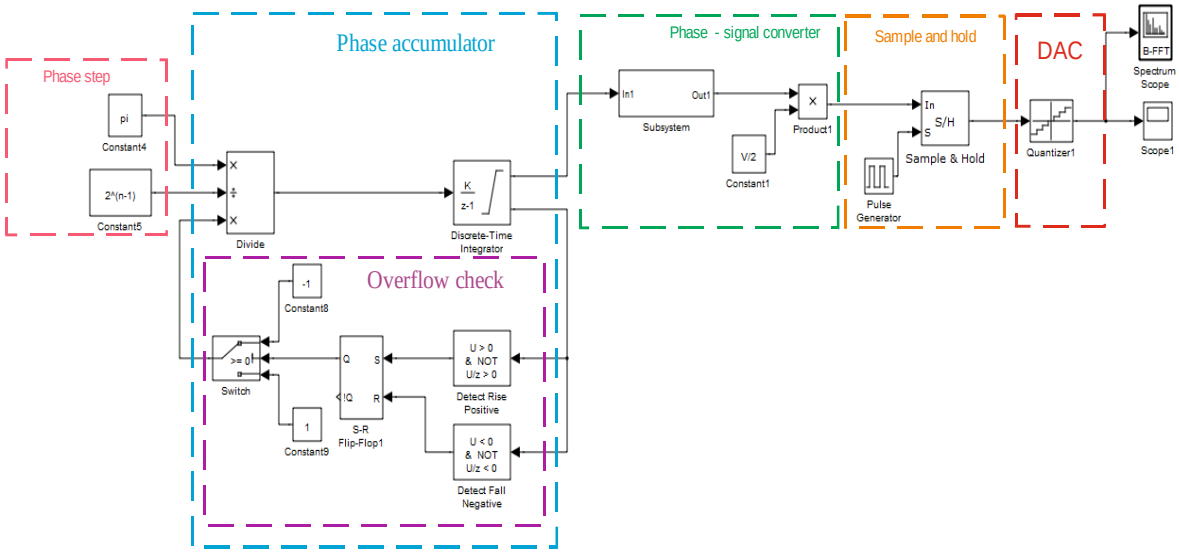


Fig. 2 Simulink model of digital signal processor for series based DDS with optimized 5th order polynomial

In the phase to signal converter the polynomial approximation of the sine function is defined. In the current paper the equation (1) is implemented with the following coefficients a3=0.16585470; a5=0.00758128. These coefficients allow a generation of a sine wave with SFDR of 91,4dB [5] without considering the influence of the DAC.

2. Simulation results

An example of the operation of the developed model is represented below. Figure 3 shows the phase accumulation. Together with Figure 4 they present the work of the DDS with the influence of the signal processor or DAC. Figure 5 represents the processing of the generated signal by including the working frequency of the microprocessor, which is 80MHz. The time for instruction execution and leading out the values to the output port is experimentally defined to be 1μs for microcontroller PIC32MX460F512L. The SFDR in this case is 56dB and is presented in figure 7a.

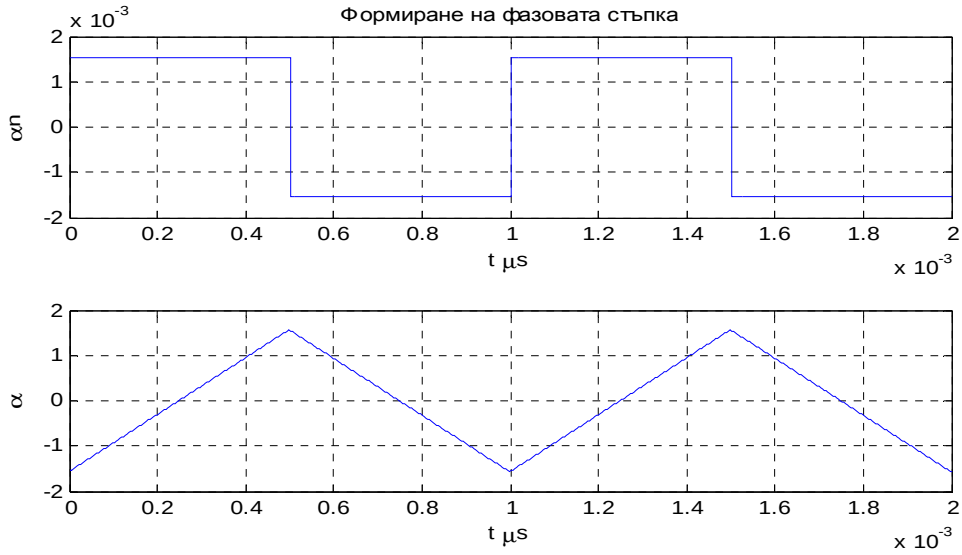


Fig. 3 Phase step forming and accumulated phase signal

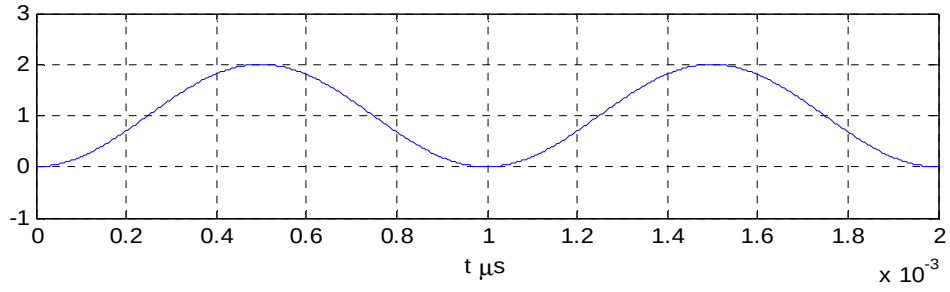


Fig. 4 Output signal of phase-signal converter

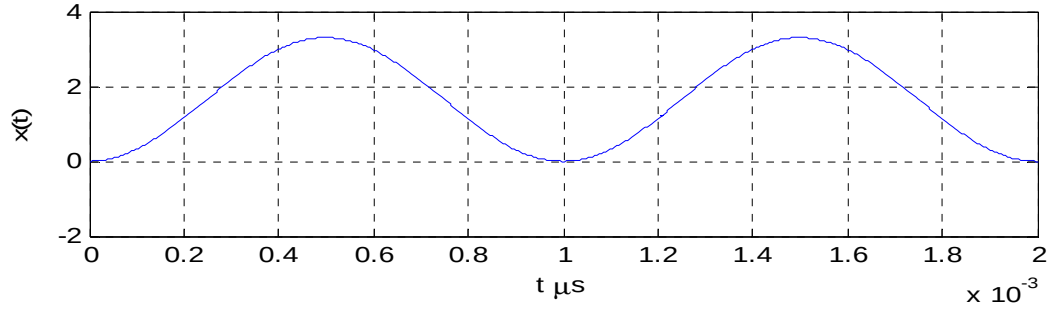


Fig. 5 Signal processing with a working frequency of the microprocessor of 80MHz

Figure 6 presents the work of the model when the time is lower than the needed for calculating and leading out the output signal. In this case the defined time is 10 µs, experimentally defined for the working frequency of 8MHz for PIC32MX460F512L.

The frequency spectrum of the output signal is calculated and the dynamic range is defined to be 34,5dB (figure 7b).

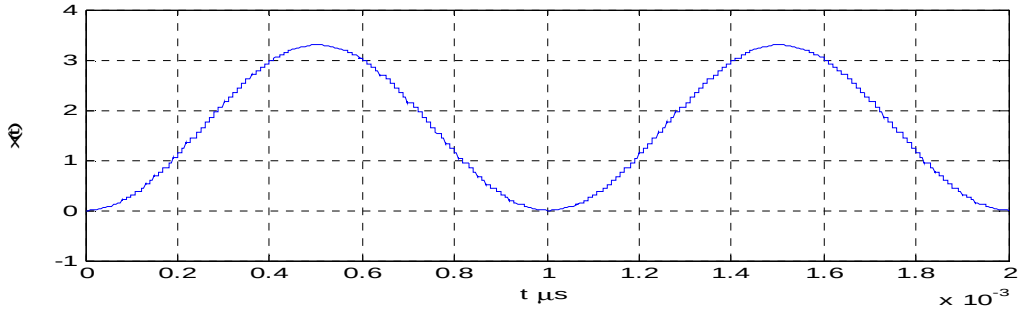
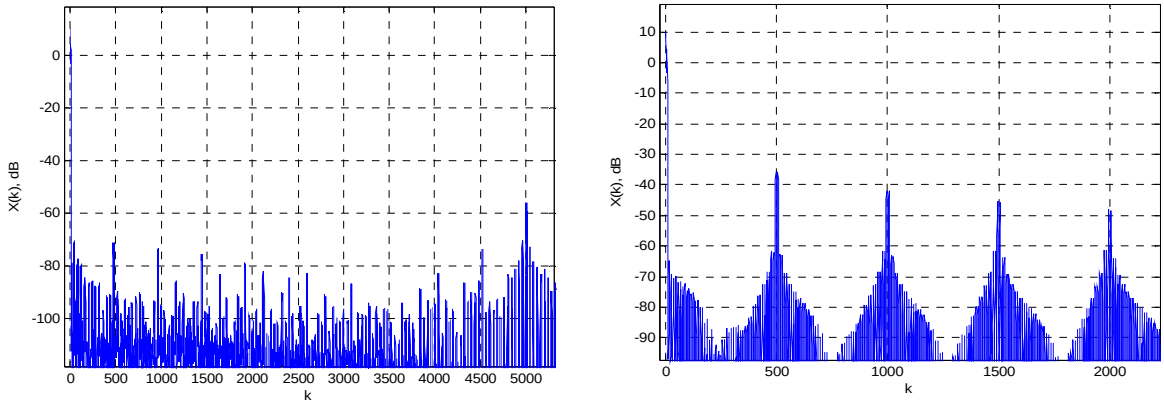


Fig. 6 Signal processing with a working frequency of the microprocessor of 8MHz



a) *b)*

Fig. 7 Spectrum of the output signal using microprocessor with working frequency of a) 80MHz and b) 8MHz respectively.

Running the simulation with DAC resolution of 12 bits gives a SFDR of the output signal 70dB. Increasing of the DAC resolution from 6 to 16 bits the quantization error in the output signal decreases all together with the level of the side spectra components with resides in higher SDFR. However due to restrictions in the implementation not always a high working frequency and high DAC resolution can be used.

Conclusions

The current paper presents a dedicated computer based model for implementing series based DDS algorithms. The model is tested on simulations based on experimentally obtained microcontroller data. The obtained results suggest that the model can be useful when testing and

evaluating the parameters of different algorithms. It allows the analyzing of the signal processing in the DDS implemented so a conclusion about the work for the chosen microcontroller could be made.

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